Remarks

The final Office Action dated September 29, 2009 notes the following rejections: claims 1-20 stand rejected under 35 U.S.C. § 103(a) over Hennessy ("Computer Organization and Design: The Hardware/Software Interface") in view of Colwell (U.S. Patent No. 5,604,878). Applicant traverses the rejection and, unless explicitly stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Office Action.

Applicant respectfully traverses the § 103(a) rejection of claims 1-20 because the cited Hennessy reference either alone or in combination with the '878 reference lacks correspondence to the claimed invention. For example, the claimed invention requires that the latch is held open for the generated pipeline data to propagate through the latch in the reduced mode; however, such aspects are not taught by either of the cited references. Because neither reference teaches these aspects, no reasonable interpretation of the asserted prior art, taken alone or in combination, can provide correspondence. As such, the rejections fail.

More specifically, the Hennessy reference does not teach that the MEM/WB stage (*i.e.*, the asserted latch) is bypassed in a reduced mode, as acknowledged by the Examiner (*see, e.g.*, page 3 of the instant Office Action). The '878 reference, however, teaches bypassing a pipe extend buffer 60 in a manner that does not involve data propagating through the buffer 60. *See, e.g.*, Figure 3 and Col. 7:55-62. Instead, the data is routed without passing through the buffer 60 as is shown in Figure 3. As such, the Examiner fails to cite to any reference that teaches that a latch is held open for the generated pipeline data to propagate through the latch in the reduced mode (as claimed). In an apparent recognition of the lack of correspondence and in the failed attempt to maintain the rejection, the Examiner asserts that one way "to allow for early retirement ... would be to allow the MEM/WB pipeline register to be keep open ...which allows for the ALU result to flow out of the MEM/WB pipeline register (*see* page 12 of the instant Office Action). However, as the Examiner fails to cite to any reference that teaches keeping MEM/WB pipeline register open to allow data to propagate through the register, the rejection necessarily fails and must be withdrawn. Application further submits that the

Examiner is improperly attempting to modify the Hennessy reference in a manner that is taught, not by the cited references, but by Applicant, in a blatantly improper hindsight reconstruction of the claimed invention using Applicant's disclosure as a template. *See, e.g.,* M.P.E.P. § 2142.

In addition, the Examiner fails to cite to any reference that teaches a reduced mode of operation, as in the claimed invention. The Examiner acknowledges that the Hennessy reference does not teach operation in a reduced mode that bypasses a processing stage of a pipeline, as discussed above. The '878 reference also fails to teach a reduced mode that bypasses a processing stage of a pipeline. Instead, the '878 reference teaches that a pipe extend buffer 60 is added after the end of the third pipe stage 43 of the unit. *See, e.g.,* Figure 3. The '878 reference uses the buffer 60 to extend the length of the pipeline when writeback conflict exists. *See, e.g.,* Col. 7:55-66. As such, the '878 reference teaches a normal mode and an extended mode, not a reduced mode as erroneously asserted by the Examiner.

In view of the above, the § 103 rejection is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 103 rejection of claims 1-20 because the Examiner's proposed modification of the Hennessy reference undermines the operation of Hennessy. Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main (Hennessy) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (U.S. 2007). ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). In this instance, the Examiner proposes to modify the Hennessy reference such that MUX 61 and control logic 62 of the '878 reference (*see* Figure 3) are used to bypass MEM/WB stage of Hennessy's pipelined datapath (*see* Figure 6.25). However, as asserted by the Examiner, Hennessy is directed to a synchronous pipeline processor that is controlled by a clock signal. The Hennessy reference requires MEM/WB to ensure synchronization of the data being processed by the pipeline. As such, bypassing MEM/WB stage (asserted

by the Examiner to be a latch) would result in the corruption of the data being processed by Hennessy's synchronous pipeline processor. Accordingly, the Examiner's proposed modification would render Hennessy inoperable.

In response to Applicant's previous arguments regarding the impropriety of the proposed modification of Hennessy, the Examiner mischaracterizes the teachings of the '878 reference in a failed attempt to maintain the rejection. Specifically, the Examiner erroneously asserts that "(w)hen the ALU instruction reaches the fourth pipeline stage, the control logic of Colwell (the '878 reference) determines that no conflict occurs in the fifth pipeline stage and that the ALU instruction can wire its data a clock cycle early to the register file" (*see* page 11 of the instant Office Action). The '878 reference, however, does not teach that the control logic 62 allows for bypassing pipeline stages in the middle of Hennessey's synchronous pipeline processor. Instead, the '878 reference teaches that a pipe extend buffer 60 is added after the end of the third pipe stage 43 of the unit to extend the pipeline. *See, e.g.,* Figure 3. The '878 reference uses the buffer 60 and the control logic 62 to extend the length of the pipeline when writeback conflict exists. *See, e.g.,* Col. 7:55-66. As such, the '878 reference's control logic 62 does not make a determination that would allow for bypassing the MEM/WB stage in the middle of Hennessey's synchronous pipeline processor. Accordingly, the proposed combination would result in the corruption of the data being processed by Hennessy's synchronous pipeline processor.

In view of the above, the Hennessy reference teaches away from the Examiner's proposed modification and there is no motivation for the skilled artisan to modify Hennessy in such a manner. Therefore, the § 103 rejection is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 103 rejection of claims 2 and 3 because the proposed combination does not correspond to aspects of the claimed invention directed to a latch control circuit configured to provide an enable signal to the latch in the normal mode and to prevent the enable signal from being provided to the latch in the reduced mode. The '878 reference does not teach that control logic 60 (*i.e.,* the asserted latch control circuit) provides any signals to buffer 60. Instead, the control logic 62 provides a

control signal to MUX 61 to select the desired output. Accordingly, the § 103 rejection of claims 2-3 is improper and Applicant requests that it be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Juergen Krause-Polstorff, of NXP Corporation at (408) 474-9062 (or the undersigned).

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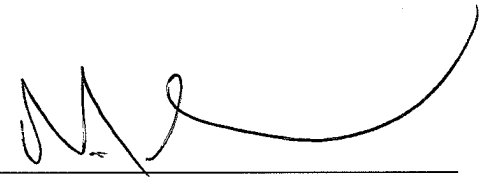
By: 

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